IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 6 with the following paragraph:

1) Serial No. ~~[Docket No. 00-BN-051]~~ 09/751,372, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR";

Please replace the paragraph beginning on page 6, line 10 with the following paragraph:

2) Serial No. ~~[Docket No. 00-BN-052]~~ 09/751,331, filed concurrently herewith, entitled "PROCESSOR PIPELINE STALL APPARATUS AND METHOD OF OPERATION";

Please replace the paragraph beginning on page 6, line 13 with the following paragraph:

3) Serial No. ~~[Docket No. 00-BN-053]~~ 09/751,371, issued as U.S. Patent No. 6,691,210, filed concurrently herewith, entitled "CIRCUIT AND METHOD FOR HARDWARE-ASSISTED SOFTWARE FLUSHING OF DATA AND INSTRUCTION CACHES";

Please replace the paragraph beginning on page 6, line 17 with the following paragraph:

4) Serial No. ~~[Docket No. 00-BN-054]~~ 09/751,327, filed concurrently herewith, entitled "CIRCUIT AND METHOD FOR SUPPORTING MISALIGNED ACCESSES IN THE PRESENCE OF SPECULATIVE LOAD INSTRUCTIONS";

Please replace the paragraph beginning on page 6, line 21 and ending on page 7, line 2 with the following paragraph:

5) Serial No. ~~[Docket No. 00-BN-055]~~ 09/751,377, filed concurrently herewith, entitled "BYPASS CIRCUITRY FOR USE IN A PIPELINED PROCESSOR";

Please replace the paragraph beginning on page 7, line 3 with the following paragraph:

6) Serial No. ~~[Docket No. 00-BN-056]~~ 09/751,410, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR EXECUTING CONDITIONAL BRANCH INSTRUCTIONS IN A DATA PROCESSOR";

Please replace the paragraph beginning on page 7, line 7 with the following paragraph:

7) Serial No. ~~[Docket No. 00-BN-057]~~ 09/751,408, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ENCODING CONSTANT OPERANDS IN A WIDE ISSUE PROCESSOR";

Please replace the paragraph beginning on page 7, line 10 with the following paragraph:

8) Serial No. ~~[Docket No. 00-BN-058]~~ 09/751,330, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SUPPORTING PRECISE EXCEPTIONS IN A DATA PROCESSOR HAVING A CLUSTERED ARCHITECTURE";

Please replace the paragraph beginning on page 7, line 14 with the following paragraph:

9) Serial No. ~~[Docket No. 00-BN-066]~~ 09/751,678, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION IN A DATA PROCESSOR HAVING A CLUSTERED ARCHITECTURE"; and

Please replace the paragraph beginning on page 7, line 18 with the following paragraph:

10) Serial No. ~~[Docket No. 00-BN-067]~~ 09/751,679, filed concurrently herewith, entitled "INSTRUCTION FETCH APPARATUS FOR WIDE ISSUE PROCESSORS AND METHOD OF OPERATION".

Please replace the paragraph beginning on page 22, line 12 with the following paragraph:

Instructions are issued to an operand read stage associated with register file 310 and then propagated to the execution units (i.e., integer units ~~341-244~~ 341-344, multipliers 351-352). Cluster 220 accepts one bundle comprising one to four syllables in each cycle. The bundle may consist of any combination of four integer operations, two multiplication operations, one memory operation (i.e., read or write) and one branch operation. Operations that require long immediates (constants) require two syllables.